CLAIMS

What is claimed is:

1. A semiconductor device assembly, comprising:

a first semiconductor device including a surface with a plurality of peripherally located bond pads;

a rerouting element positioned over said first semiconductor device, said rerouting element comprising:

a base substrate;

a plurality of conductive vias positioned adjacent at least two peripheral edges of said base substrate, each conductive via of said plurality of conductive vias being located so as to align with a corresponding, peripherally located bond pad of the semiconductor device upon assembly of said rerouting element with the semiconductor device;

a plurality of conductive traces; and

a plurality of rerouted bond pads, each conductive trace of said plurality of conductive traces extending from a corresponding conductive via toward at least one other peripheral edge of said base substrate to a corresponding rerouted bond pad of said plurality of rerouted bond pads; and

a second semiconductor device positioned over a portion of said rerouting element, each of said plurality of rerouted bond pads being exposed beyond a periphery of said rerouting element.

2. The semiconductor device assembly of claim 1, wherein each rerouted bond pad of said plurality of rerouted bond pads is located laterally adjacent a periphery of said first semiconductor device.

3. The semiconductor device assembly of claim 1, wherein each rerouted bond pad of said plurality of rerouted bond pads is located adjacent a single edge of said first semiconductor device.

4. The semiconductor device assembly of claim 1, further comprising:
a carrier substrate.

5. The semiconductor device assembly of claim 4, wherein said first semiconductor device is secured to said carrier substrate.

6. The semiconductor device assembly of claim 4, wherein said carrier substrate comprises at least one of a circuit board, an interposer, another semiconductor device, and leads.

7. The semiconductor device assembly of claim 4, wherein said at least one rerouted bond pad is in communication with a corresponding contact area of said carrier substrate.

8. The semiconductor device assembly of claim 7, further comprising:
a discrete conductive element positioned between said at least one rerouted bond pad and said corresponding contact area.

9. The semiconductor device assembly of claim 8, wherein said at least one discrete conductive element comprises at least one of a bond wire, a tape-automated bond element trace, and a lead.

10. The semiconductor device assembly of claim 1, further comprising:
another rerouting element on a bond pad-bearing surface of said second semiconductor device.

11. The semiconductor device assembly of claim 1, wherein said second semiconductor device is oriented in staggered relation to said first semiconductor device.

12. The semiconductor device assembly of claim 1, wherein said second semiconductor device is smaller than said first semiconductor device.

13. The semiconductor device assembly of claim 1, further comprising:
at least one additional semiconductor device positioned over said second semiconductor device.

14. The semiconductor device assembly of claim 8, further comprising:
an encapsulant protecting at least portions of said first semiconductor device, said second semiconductor device, said at least one discrete conductive element, and portions of said carrier substrate located laterally adjacent outer peripheries of said first and second semiconductor devices.

15. The semiconductor device assembly of claim 14, wherein said encapsulant comprises a glob-top type encapsulant.

16. The semiconductor device assembly of claim 14, wherein said encapsulant comprises a transfer molding compound.

17. The semiconductor device assembly of claim 14, further comprising:
at least one external connective element in communication with at least one bond pad of said first semiconductor device.

18. A rerouting element for use with a semiconductor device, comprising:
a base substrate;
a plurality of conductive vias positioned adjacent at least two peripheral edges of said base substrate, each conductive via of said plurality of conductive vias being located so as to align with a corresponding, peripherally located bond pad of the semiconductor device upon assembly of said rerouting element with the semiconductor device;

a plurality of conductive traces; and

a plurality of contact pads, each conductive trace of said plurality of conductive traces extending from a corresponding conductive via toward at least one other peripheral edge of said base substrate to a corresponding contact pad of said plurality of contact pads.

19. The rerouting element of claim 18, wherein said plurality of conductive vias are positioned adjacent three peripheral edges of said base substrate.

20. The rerouting element of claim 19, wherein each contact pad of said plurality of contact pads is positioned adjacent to another, single peripheral edge of said base substrate.

21. The rerouting element of claim 18, wherein said plurality of conductive vias are positioned adjacent to two adjacent peripheral edges of said base substrate.

22. The rerouting element of claim 21, wherein each contact pad of said plurality of contact pads is positioned adjacent to at least one of two other adjacent peripheral edges of said base substrate.